Reliability Qualification Plan for LFCSP Package at STATS ChipPAC China (SCC)

QUALIFICATION PLAN			
Test	Conditions	Sample Size	Expected Completion Date
Highly Accelerated Stress Test (HAST)*	JEDEC *JESD22-A110*	**3 x 82**	April 2014
Temperature Cycle (TC)*	JEDEC *JESD22-A104*	**3 x 82**	April 2014
Autoclave (AC)*	JEDEC *JESD22-A102*	**3 x 82**	April 2014
Solder Heat Resistance (SHR)*	*ADI-0049*	**3 x 11**	April 2014
High Temperature Storage (HTS)	JEDEC *JESD22-A103*	**1 x 82**	April 2014
Field Induced Charged Device Model (FICDM)	JEDEC *JESD22-C101*	**3/Voltage**	April 2014

*These samples will be subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125ºC, Soak: Unbiased Soak: 192 hrs @ 30ºC, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260ºC.